

INDUSTRY NEWS

California colleges, industry team to explore post-CMOS frontier



TERRA INCOGNITA: Kang Wang of UCLA's School of Engineering and Applied Science says that WIN will focus on spin logic devices, device coupling and circuits, and metrics and benchmarks. (PHOTO BY IRENE FERTIK, COURTESY OF UCLA SCHOOL OF ENGINEERING AND APPLIED SCIENCE)

One of the newest outposts on the post-CMOS frontier is located in a tight cluster of classroom buildings on the southern part of the University of California Los Angeles campus. The engineering school there will house the headquarters of an ambitious new research project to explore terra incognita at the far reaches of the semiconductor industry's technology roadmap.

Launched in March, the Western Institute of Nanoelectronics (WIN) links UCLA with three other California universities and six industrial sponsors in a program that will initially examine the use of

spintronics for semiconductor manufacturing. The participants say the technology, developed by French and German physicists in 1988, is the most promising of several nontraditional methods for making devices with feature sizes well below 65 nm.

In addition to UCLA, the participating universities that will comanage WIN are UC Berkeley, UC Santa Barbara, and Stanford. The industrial sponsors are AMD, Freescale Semiconductor, IBM, Intel, Micron Technology, and Texas Instruments. To help the launch, Intel has offered an equipment grant of \$10 million, and at least 10 researchers from the device makers will work with students and faculty. The \$10 million will be divided equally among the four universities.

The program begins with solid if not extravagant financial backing. WIN has received starting grants totaling \$18.2 million and grants of \$14.38 million from its industrial partners. In addition, California's Industry-University Cooperative Research Program has offered a matching UC Discovery Grant of \$3.84 million. WIN will receive the money over a four-year period. UCLA notes that personnel—at least 30 top-notch researchers will take part—and infrastructure support from the participating universities are worth an estimated \$200 million.

Kang Wang will direct this cooperative effort from his airy office in UCLA's Henry Samueli School of Engineering and Applied Science. The office windows overlook the bustle of construction surrounding two buildings that, when opened later in 2006, will become an integral part of the new center's explorations. One will house the California NanoSystems Institute (CNSI), a statewide initiative that will provide 6000 sq ft of R&D space for WIN and its precursor, and now its partner, the Center on Functional Engineered Nano Architectonics (FENA).

A veteran engineering professor at UCLA and director of FENA, the bespectacled Wang is an enthusiastic proponent of WIN's work in spintronics. The institute has three focus areas with three themes, he says. The first is spin logic devices, the second is device coupling and circuits, and the third is metrics and benchmarks. Benchmarking means, "are [the devices] good compared with scaled CMOS?" Lead researchers at UCSB jointly with UC Berkeley and Stanford will oversee the first and second focus areas, respectively, with UCLA handling the third.

During a recent interview and site tour, Wang described several challenges that WIN must tackle in order to fulfill the institute's mission of finding a solution by 2020. The institute plans to explore spintronics' promise for the next four or five years and then evaluate the progress made before deciding whether to pursue other technological paths, such as nanophotonics. He says one key factor will determine the institute's research approach.

“Scalability is the important thing, because information processing requires billions or even trillions of things working together to reach so-called throughput. That’s why the important thing about the approach is, is it scalable?”

Known also as magnetoelectronics, spintronics works by using the spin of an electron, instead of its electrical charge, to move information within circuits. The technology’s low power consumption and subsequent heat dissipation is particularly attractive to semiconductor manufacturers. The technology harnesses this electron spin into an uninterrupted chain of motion.

In experimental work at UC Santa Barbara, David Awschalom, the director of the university’s Center for Spintronics and Quantum Computation Processing and a lead WIN researcher, has already shown that an aligned swarm of spinning electrons can transport information. IBM has pioneered research in the field, particularly involving giant magnetoresistive (GMR) read-heads. Magnetic RAM devices, or MRAMs, have also shown great commercial promise, according to reports.

As the name indicates, MRAMs utilize the ability of spinning electrons to act as switches. In WIN’s case, the researchers are looking to develop a working logic device. Wang says spintronics works like this: “If the spin goes up, it’s one; spin goes down, it’s zero, and you learn how to define it as a logic state.”

By definition, spintronics introduces magnetic atoms such as manganese, cobalt, and iron into the process, he points out. Naturally, this prospect gives process engineers the willies. “In the front end, you really don’t like those elements. In standard microelectronics [manufacturing] people really do not want to have...all these magnetic and transition metals.”

Process control—what else?—is crucial to handling these metals. “One has to learn how to control it without degradation,” Wang says. “If this device is to work with CMOS on a semiconductor platform, one will have to worry about how they work together. Obviously, with temperature control and being confined to a small area by nanostructures, the most important thing we have to see is how will [the metals] be compatible with front-end processes. Back end is no problem.”

“Basically, what our sponsors are asking us to do is invent something new here,” says Jeff Bokor, a professor of electrical engineering and computer science at UC Berkeley and the WIN principal investigator for the university. “That’s actually one of the more interesting aspects of this. Typically, universities come up with inventions, and then we go get sponsors to go out and develop them. This one didn’t go that way. These sponsors approached us.”

Some of the investigators have been active in GMR and MRAM technology, Bokor points out. "The key thing is this: Our sponsors are saying, 'we see what's going on in those technologies, MRAM is getting close to commercial product. So basically, they've challenged us and asked us, 'can you adapt this technology, extend it, or expand it somehow to make logic devices?'"

The low-power aspect intrigues the sponsors. The energy needed to trigger a gate in a CMOS-based device relates to the amount of current and input capacitance, Bokor notes. "So the energy you have to dissipate in a logic gate is the energy it takes to charge up the input capacitance. We're moving charge around."

In a spintronic device much less energy may be needed to flip a spin to an on or off state. "That at least has the potential to be considerably smaller, and, we hope, with the same degree of noise immunity and those other good things," he says. "It's a big question mark, but that's the challenge. We're probably not talking about logic devices in which we encode the information in one single spin. It'll probably be a collection of spins. But we're open [to exploring all our options]." The next logic device or switch could be based on a completely new technology or a technology that could be integrated with CMOS, researchers say.

For conventional MRAM spintronics "it is nanomagnetism, essentially," explains Hans Coufal, director of the Nanoelectronics Research Corp. (NERC), which is one of the key backers of WIN through the Nanoelectronics Research Initiative (NRI). "In spintronics, what NRI is really after is trying to use spin to carry information. It's still relatively theoretical."

Coufal says participants will know more by the end of 2006 about what is viable and what is not. It's too soon, he insists, to consider one of the main concerns of every chipmaker. "We are not concerned about yields yet," he replies in answer to a question. "We believe that with very small things you will have to learn how to build a perfect system with imperfect components."

The beauty of WIN is that "it brings together some of the very best West Coast universities and gets faculty and students to talk together about problems near and dear to my heart, which is post-CMOS logic," says Coufal, who has ties to IBM's Almaden Research Center in San Jose. The institute also takes advantage of existing and underutilized infrastructure, such as the California Nanosystems Institute and the recently dedicated new molecular foundry at Lawrence Berkeley National Lab.

Echoing Bokor's comments, the NERC director points to WIN's 15-year time horizon, adding that WIN's work is unlike the normal research scenario, "where you pay somebody to get a job done for you and deliver data. This is really high-risk research."

WIN's participants risk the possibility "that none of the devices will work," Coufal notes. Or they'll discover that the answer is this device or that device. "We want to make sure that we leave no stone unturned."

Because of the exotic metals involved, the research will require tools that go beyond the usual process gear. "Some of the deposition equipment may be exotic," Coufal says. Nanoimprinting may be used in place of conventional photo-lithography, and directed self-assembly is also being considered.

Kos Galatsis, COO of WIN, explains that the sponsors have left it primarily up to the universities to develop a wish list of the equipment "that will complement our technical agenda here." That list includes gear specifically for spintronics. "One is magnetic force microscopy, or MFM. Another one we're looking at getting is PPMS, or physical property measurement system." The system "can vary temperature, it can vary magnetic field, and it can characterize the sample within the chamber."

Wang adds that WIN is considering construction of a facility "that can measure single spin." He also expects to obtain more E-beam writing and nanoimprinting capabilities. "The nano-imprinting facility will facilitate our research program because we can produce nanopatterns readily. Like E-beam, it writes well, but it writes slowly, so we don't have as many samples produced, and therefore it's much more economical to do research." It's important for WIN to produce "a lot of different processes and different nanostructures."

"Typically, for research purposes we're not going to be using 12- or even 8-in. wafers," Coufal says. "That doesn't make sense for research." The participants will use "relatively small wafers for fast learning and rapid throughput."

On a walking tour of the engineering and science buildings that takes a visitor across interconnecting bridges and up and down stairs and across the Science Court to several labs, Wang notes that he personally established the nanoelectronics facility in 1989, pointing out its E-beam, patterning, deposition, sputtering, and molecular beam epitaxy systems. The MBE tool is used for depositing germanium and manganese germanium. The cleanrooms are Class 1000 with Class 100 chases, typical for a university facility, he says. He set up his own research lab "in the last 20 years or so," using contracts and research grants into silicon germanium and other III-V compounds.

Alexander Khitun, a research engineer in the electrical engineering department's Device Research Laboratory, is one of WIN's coprincipal investigators. Introduced during the tour, he says he has worked with Wang, his boss, for almost seven years on spin waves and logic devices. Khitun notes that his research "is an entirely new

approach developed by our lab and our group.” The group submitted several patent applications to the UCLA intellectual property office and recently received a patent award.

This solid bit of groundwork and the level of cooperation already established fuel much of the optimism shared by Wang and the other research participants. “One of the important elements in WIN’s overall approach is that all four campuses have diverse programs in electronics technology,” Bokor points out.

The WIN research model’s uniqueness stems from the fact that industry is heavily participating in that effort. Initially, industry participated in the scope definition and proposal generation and coordinated the delivery of the proposal and the support material. Then once WIN is established, industry will contribute at three different levels: providing the expertise for supporting WIN’s technical and nontechnical needs; providing the equipment needed for that research; and providing the cash to support WIN researchers across different campuses.

What would be the equivalent of spun-gold for WIN’s research efforts? “If we have a...logic switch using spin,” replies Coufal. “That’s about the maximum you can expect in a couple of years.”—
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